

Navid Azizi

Education	Jan. '03 – Current	University of Toronto	Toronto, Ontario
	Ph.D.		
		<ul style="list-style-type: none">▪ Ph.D. Thesis: Challenges in Nanometre Digital Integrated Circuit Design<ul style="list-style-type: none">▪ Includes work on reducing leakage in SRAM and FPGA structures, reducing the SER in memories, analyzing the effects (delay, leakage) of process variations on circuits, and using circuit techniques to reduce the effect of variations.▪ Expected defence date: April 2007	
	Sept. '01 – Oct. '02	University of Toronto	Toronto, Ontario
	Master's of Applied Science		
		<ul style="list-style-type: none">▪ Master's Thesis: Low Leakage Asymmetric-Cell SRAM<ul style="list-style-type: none">▪ Developed a low-leakage SRAM cell by using an asymmetric configuration of high-Vt transistors, which in conjunction with a new sense amplifier did not affect performance	
	Sept. '98 – May '01	University of Toronto	Toronto, Ontario
	Bachelor of Computer Engineering		
		<ul style="list-style-type: none">▪ Received B.A.Sc degree with a CGPA of 3.94.▪ Ranked 1st overall in program	
Work experience	Jan. '02 – Dec. '06	University of Toronto	Toronto, Ontario
	Head Teaching Assistant		
		<ul style="list-style-type: none">▪ Head TA for ECE451, VLSI Systems (fourth year class) for 150-200 students▪ Developed lab material, provided support for lab design activities	
	Jun '05 – Sep. '05	Intel, Circuits research labs	Hillsboro, Oregon
	Electronics Engineer		
		<ul style="list-style-type: none">▪ Worked on compensation of process variations at very low voltages.	
	May '04 – Aug. '04	Intel, Circuits research labs	Hillsboro, Oregon
	Electronics Engineer		
		<ul style="list-style-type: none">▪ Worked on statistical low-voltage techniques in the presence of process variations.	
	July '02 – Aug. '02	Texas Instruments, SRAM design group	Dallas, Texas
	Electronics Engineer		
		<ul style="list-style-type: none">▪ Designed asymmetrical SRAM designs in various processes	
	Summer '00 and '01	Altera Canada, Toronto Technology Centre	Toronto, Ontario
	Software Engineer		
		<ul style="list-style-type: none">▪ Designed a portion of the fitter to hierarchically size regions within a design and to initially place them.▪ Worked on project to implement incremental compile, and a modular design flow in existing Altera software tools.	

Publications

Journal papers

1. N. Azizi, M.M. Khellah, V. De, and F.N. Najm. Variations-aware low-power design and block clustering with voltage scaling. Submitted to *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, May 2006.
2. A. Moshovos, B. Falsafi, F.N. Najm and N. Azizi. A case for asymmetric-cell cache memories. *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 13(7):877-881, July 2005.
3. N. Azizi, F.N. Najm, and A. Moshovos. Low-leakage asymmetric-cell SRAM. *IEEE Trans. on Very Large Scale Integration Systems (TVLSI)*, 11(4):701-715, August 2003.

Conference proceedings

1. K. Pagiamtzis, N. Azizi, and F.N. Najm. A Soft-Error Tolerant Content-Addressable Memory (CAM) Using An Error-Correcting-Match Scheme. *IEEE Custom Integrated Circuits Conference (CICC)*, pages 301-304, September 2006.
2. N. Azizi and F.N. Najm. A family of cells to reduce the soft-error-rate in ternary-CAM. *ACM/IEEE Design Automation Conference (DAC)*, pages 779-784, July 2006.
3. G. Nabaa, N. Azizi and F. N. Najm. An adaptive FPGA architecture with process variation compensation and reduced leakage. *ACM/IEEE Design Automation Conference (DAC)*, pages 624-629, July 2006.
4. N. Azizi and F.N. Najm. Look-up table leakage reduction for FPGAs. *IEEE Custom Integrated Circuits Conference (CICC)*, pages 186-189, September 2005.
5. N. Azizi and F.N. Najm. Compensation for within-die variations in dynamic logic by using body-bias. *IEEE North-East Workshop on Circuits and Systems (NEWCAS)*, pages 167-170, June 2005.
6. N. Azizi, M.M. Khellah, V. De, and F.N. Najm. Variations-aware low-power design with voltage scaling. *ACM/IEEE Design Automation Conference (DAC)*, pages 529-534, June 2005.
7. N. Azizi, I. Kuon, A. Egier, A. Daribiha, P. Chow. Reconfigurable Molecular Dynamics Simulator. *IEEE International. Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 197-206, April 2004.
8. N. Azizi and F.N. Najm. An asymmetric SRAM cell to lower gate leakage. *IEEE Intl. Symposium on Quality Electronic Design (ISQED)*, pages 534-539, March 2004.
9. N. Azizi, A. Moshovos, F.N. Najm. Low-leakage asymmetric-cell SRAM. *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pages 48-51, August 2002.

Awards received

- SRC Inventor Recognition Award in 2005
- SRC Inventor Recognition Award in 2003
- NSERC CGS in 2003
- NSERC PGS in 2001
- Recipient of a University of Toronto Scholar Scholarship in 2000
- Recipient of a "Solutions Excellence" award from IBM Canada for development and implementation of the Wirebonder verification program

Patents

- N. Azizi and F.N. Najm. "Low leakage routing switch," US Provisional Patent Application, filed August 8 2005, supported by the Semiconductor Research Corporation (SRC).
- N. Azizi , F. N. Najm, and A. Moshovos. "Low Leakage Asymmetric SRAM Cell Devices," US Patent Application, supported by the Semiconductor Research Corporation (SRC).
- N. Azizi, M.M. Khellah, V. De, and Farid N. Najm. "Method for Temperature-Dependent Deactivation of Parallel Low-Voltage Circuits," US Patent Application, filed November 2004, supported by Intel Corp.

Computer Skills

- **CAD Tools:** Experienced using SPICE, Cadence, Synopsys, Altera Quartus II
- **Computer Languages:** Experienced in VHDL, Verilog, JAVA, C, C++, Perl, and sh
- **Computer Systems:** Experienced with Linux, Solaris, Windows